Analysis of Buck Converter Efficiency

Abstract

The synchronous buck circuit is wildly used to provide non-isolated power for low voltage and high current supply to system chip. To realize the power loss of synchronous buck converter and to improve efficiency is important for power designer. The application note introduces the analysis of buck converter efficiency and realizes major power component loss in synchronous buck converter.

1. Buck converter power loss analysis

To realize the power loss in converters is important for converter design optimization. Figure1 shows the general single phase synchronous buck converter circuit. The major power losses in synchronous buck converter circuit are listed as bellow :

A : Power semiconductor loss
B : Inductor loss
C : Driver loss
D : PCB trace loss

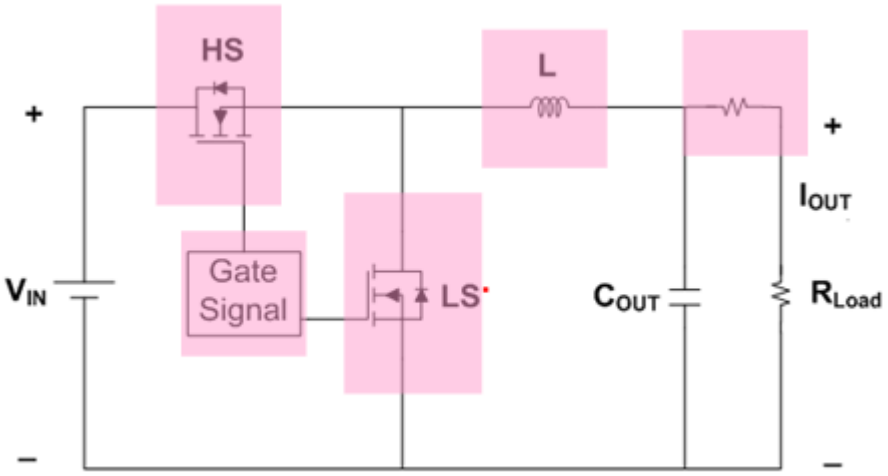

Figure 1. Synchronous buck converter

2. Power loss calculation

Low-power loss and highly efficient synchronous buck converters are in great demand for advanced micro-processors. The application note introduces and provides how to calculate the majority of power losses in a typical synchronous buck converter occur in the following components based on that the converter works in continuous conduction mode (CCM) fixed switching frequency, fixed input voltage and fixed output voltage.

A : Power semiconductor loss :

HMOS (High-Side MOSFET) summarizes to include : switching on & off and conduction loss.
LMOS (Low-Side MOSFET) summarizes to include : conduction, dead-time and reverse recovery charge loss.

HMOS switching on loss :

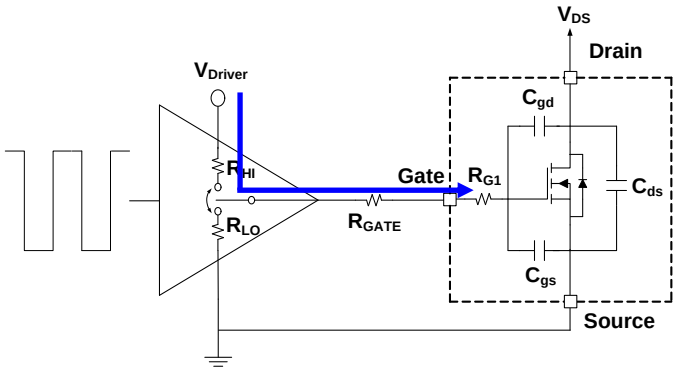

Figure 2. HMOS Driver switching on

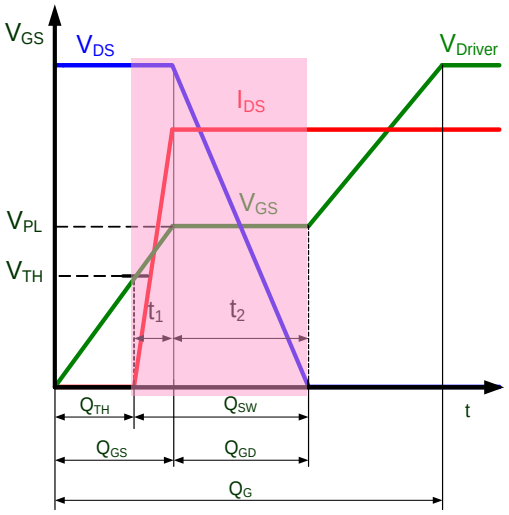

Figure 3. HMOS switching on loss area

$$P_{HS\text{-}ON} = F_{sw} \cdot V_{DS} \cdot I_{DS} \cdot \frac{t_1 + t_2}{2} = F_{sw} \cdot V_{IN} \cdot I_o \cdot \frac{T_{HS\text{-}ON}}{2}$$

$$T_{HS\text{-}ON} = \frac{Q_{SW}}{I_{G,ON}}$$

$$I_{G\text{-}ON} = \frac{V_{Driver} - V_{PL}}{R_{HI} + R_{GATE} + R_{G1}}$$

HMOS conduction loss :

The conduction loss of high-side MOSFET is determined by the on-resistances of the MOSFET and the transistor RMS current.

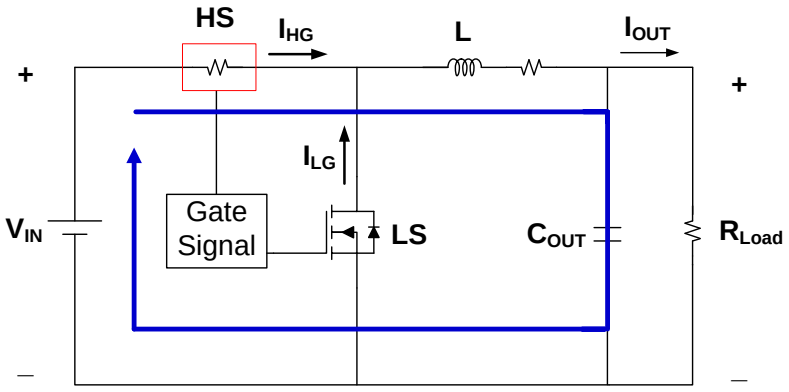

Figure 4. HMOS conduction on

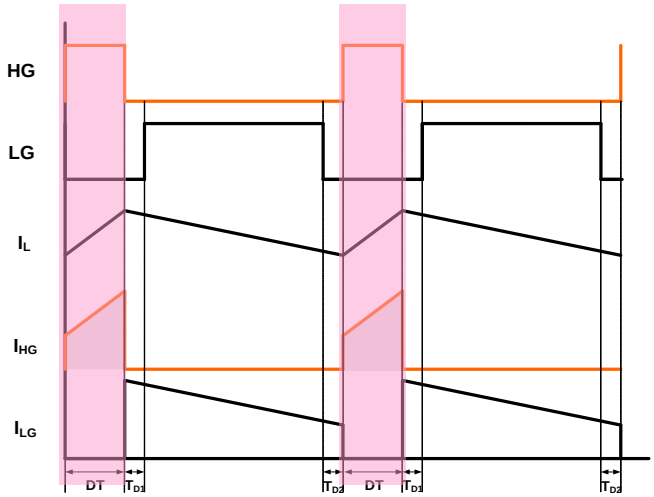

Figure 5. HMOS conduction on period

$$P_{CON\_HS} = I^2_{rms,HG} \times R_{ds(on),HS}$$

Where $I_{rms,HG} = \sqrt{D \cdot \left(I^2_{OUT} + \frac{I^2_{ripple}}{12} \right)}$

LMOS conduction loss :

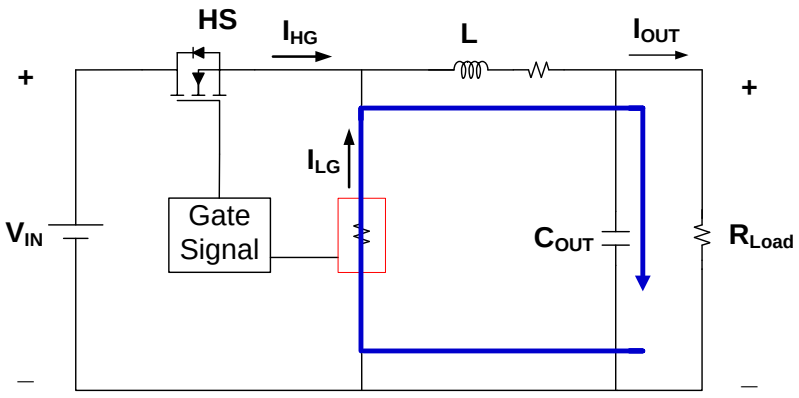

Figure 6. LMOS conduction on

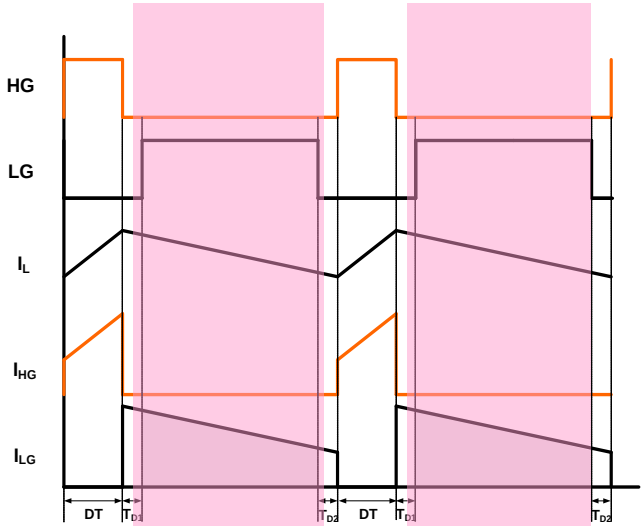

Figure 7. LMOS conduction on period

$$P_{CON\_LS} = I^2_{rms,LG} \cdot R_{ds(on),LS}$$

Where $I_{rms,LG} = \sqrt{(1\text{-}D) \cdot \left(I^2_{OUT} + \frac{I^2_{ripple}}{12} \right)}$

LMOS dead time body diode loss :

Dead-time loss is induced by LMOS body diode conduction during dead-times.

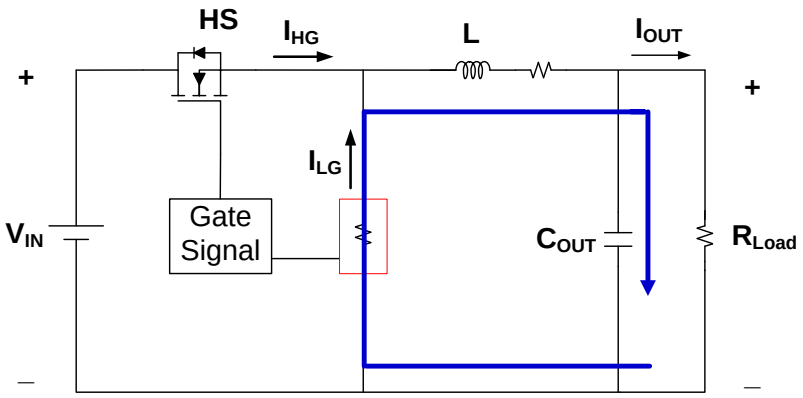

Figure 8. LMOS body diode conduction on

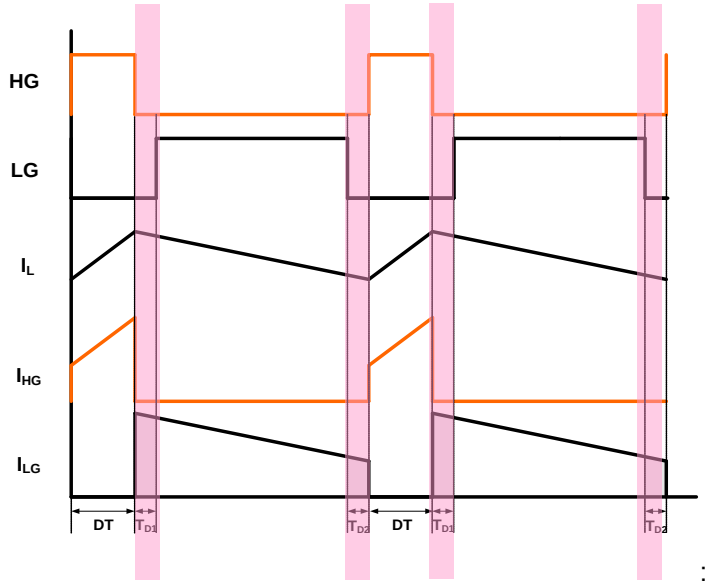

Figure 9. LMOS body diode conduction on period

$$P_{Deadtime} = V_{SD} \cdot \left[I_L \cdot T_{D2} + I_L \cdot T_{D1} \right] \cdot F_{SW}$$

$$= V_{SD} \cdot \left[\left(I_{OUT} - \frac{I_{ripple}}{2} \right) \cdot T_{D2} + \left(I_{OUT} + \frac{I_{ripple}}{2} \right) \cdot T_{D1} \right] \cdot F_{SW}$$

LMOS reverse recovery charge loss :

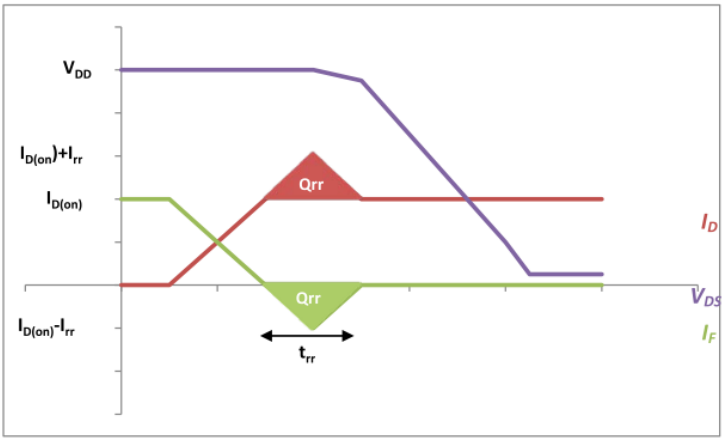

Figure 10. LMOS body diode reverse recovery period

$$P_{rr} = Q_{rr} \cdot V_{DD} \cdot F_{SW} = Q_{rr} \cdot V_{IN} \cdot F_{SW}$$

B : Inductor DC & AC loss

Inductor DC loss :

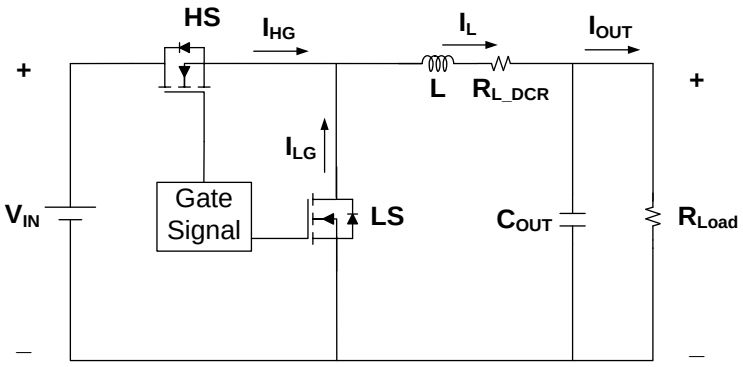

Figure 11. Current through inductor path

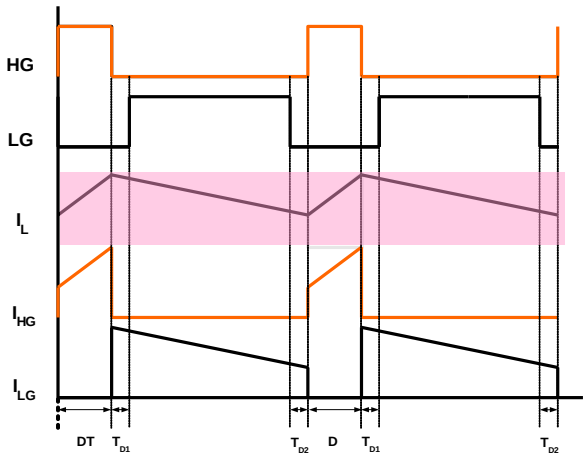

Figure 12. Inductor current path period

$$P_{copper} = I_{rms,L}^2 \cdot R_{L\_DCR}$$

Where $I_{rms,L} = \sqrt{I_{OUT}^2 + \frac{I_{ripple}^2}{12}}$

Inductor core loss :

Inductor core losses are major caused by an alternating magnetic field in the core material. The losses are a function of the operating frequency and the total magnetic flux swing. The core loss may vary from one magnetic material to another.

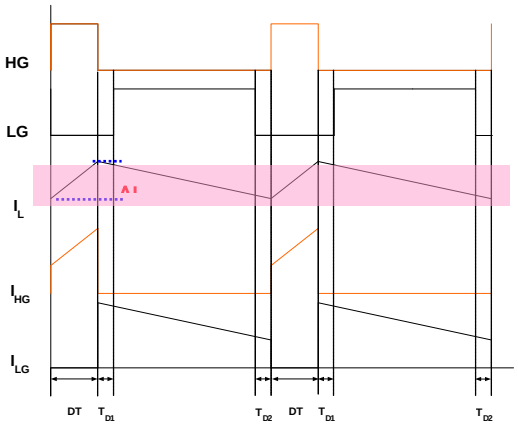

Figure 13. Inductor ripple current

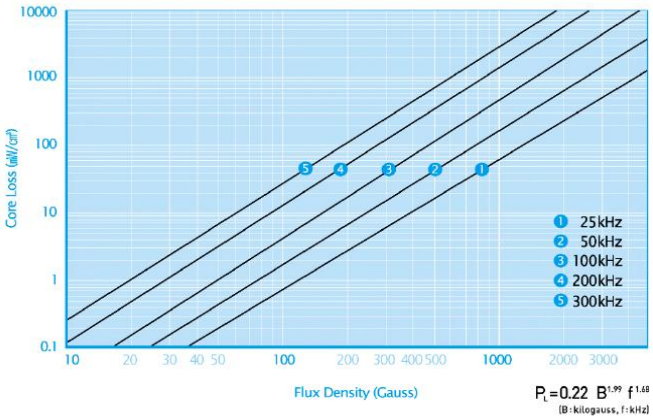

Figure 14. Core loss curve

The calculated and/or measured core loss is often directly provided by the inductor supplier. If not, a formula can be used to calculate the core loss as bellow :

$$P_L = C \cdot F_{SW}^{X} \cdot B_{max}^{Y} \cdot V_e$$

$$B_{max} = \frac{L \cdot \Delta I}{N \cdot A_e}$$

The PL is the power loss (mW),

Fsw : operating frequency

B : peak flux desity in Gauss

V_e : effective core volume

The specific value of C, X and Y are core loss parameters for each material

C: Gate driver loss :

The gate driver loss is straightforward given by MOSFET driver to charge /discharge total HMOS and LMOS Qg.

The gate driver loss is depending on MOSFET total gate charge, driver voltage and Fsw.

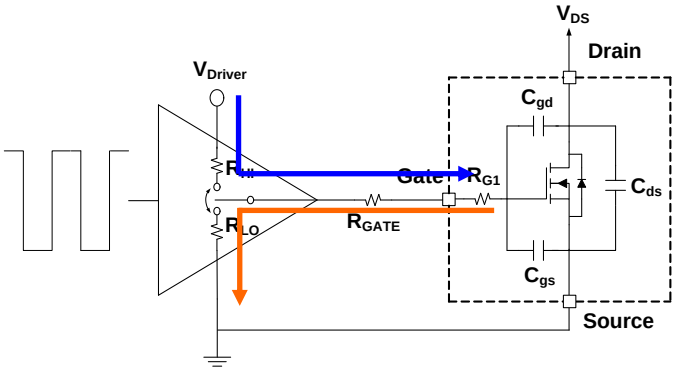

Figure 15. Driver turns on and off path

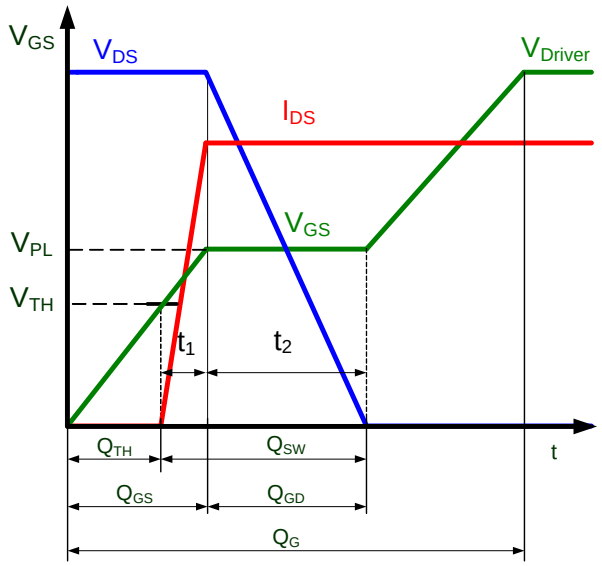

Figure 16. MOSFET driver on

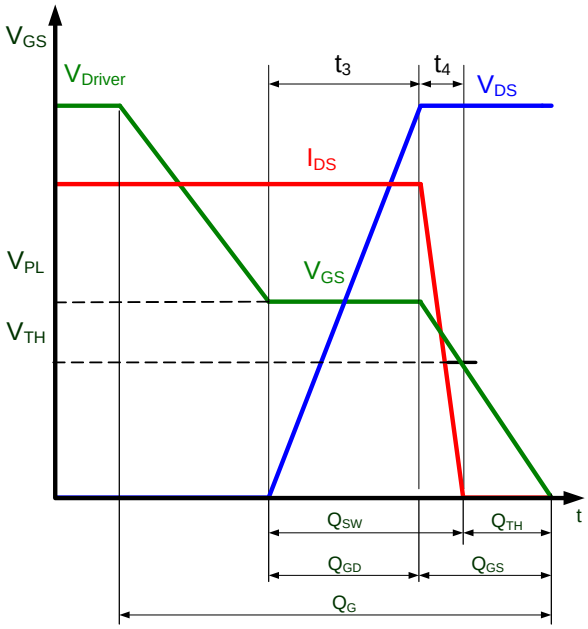

Figure 17. MOSFET driver off

$$P_{Driver} = P_{Gate(HS)} + P_{Gate(LS)}$$
$$= \left(Q_{G(HS)} + Q_{G(LS)}\right) \cdot V_{Driver} \cdot F_{SW}$$

D : PCB loss :

Figure 18 could be illustrated as Figure 19 and Figure 20 with R_{tr1}~R_{tr7} with loop1 (HMOS conduction) and loop2 (LMOS conduction) in detail.

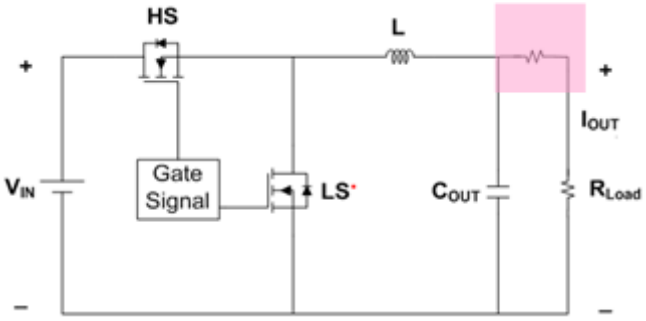

Figure 18. PCB trace diagram

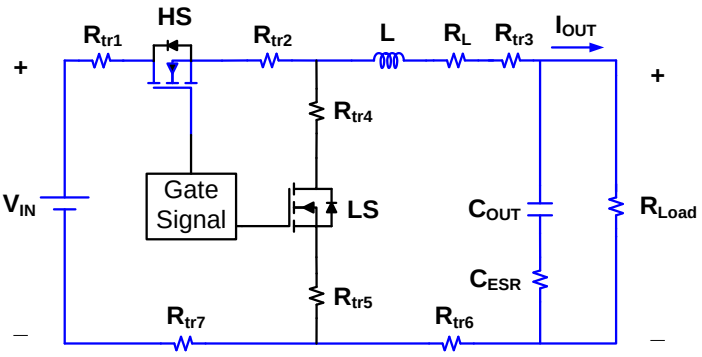

Figure 19. PCB loop1 trace

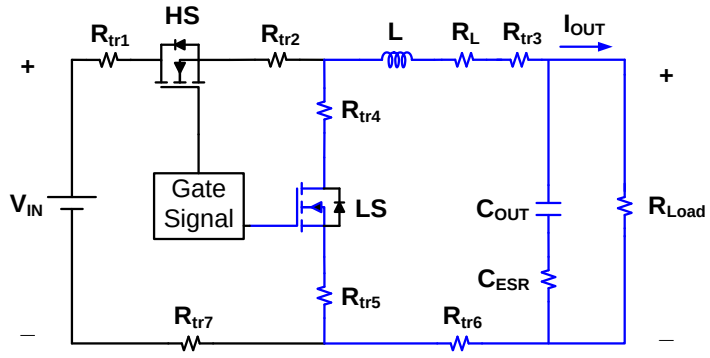

Figure 20. PCB loop2 trace

$$\text{PCB loss} = \text{PCB loop1 loss} + \text{PCB loop2 loss}$$

$$= I_{Loop1}{}^2 \times (R_{tr1} + R_{tr2} + R_{tr3} + R_{tr6} + R_{tr7}) + I_{Loop2}{}^2 \times (R_{tr3} + R_{tr4} + R_{tr5} + R_{tr6})$$

Where $I_{Loop1} = \sqrt{D \cdot \left(I_{OUT}^2 + \frac{I_{ripple}^2}{12} \right)}$

$$I_{Loop2} = \sqrt{(1-D) \cdot \left(I_{OUT}^2 + \frac{I_{ripple}^2}{12} \right)}$$

3. Power loss measurement and calculation comparison

Although the buck converter power loss calculated equations are well introduced and documented. In order to check the accuracy of these power loss equations, Table1 shows the typical buck converter application parameter and Figure 21 illustrates the efficiency comparison between measurement and calculation.

Table 1. Buck converter application parameter

IC	RT8120
VIN	12V
Vout	1.2V
FSW	300kHz
VDD	12V
L	1μH
DCR	1.2mΩ
HMOS	BSC090N03LS
LMOS	BSC090N03LS*2

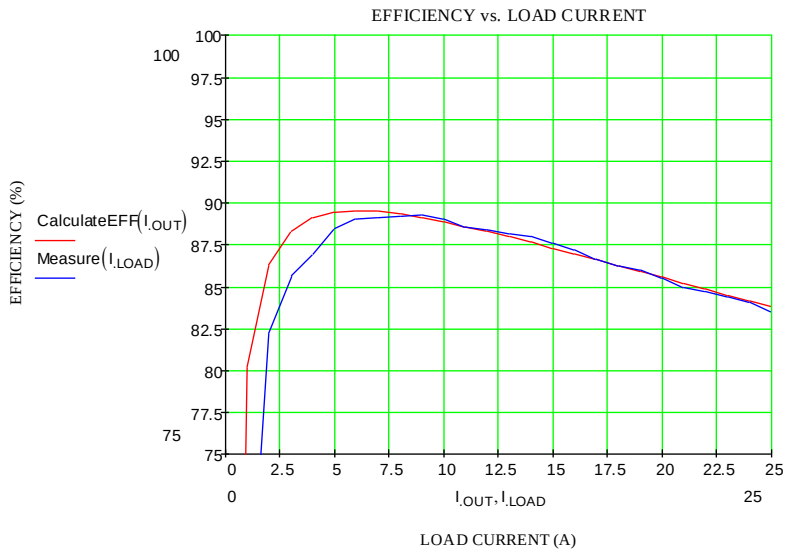

Figure 21. Measurement and calculation of efficiency comparison

Figure 22 shows the key component loss in buck converter including HMOS, LMOS, inductor, driver and PCB trace loss. Readers can check what the major loss contributed in each system loading.

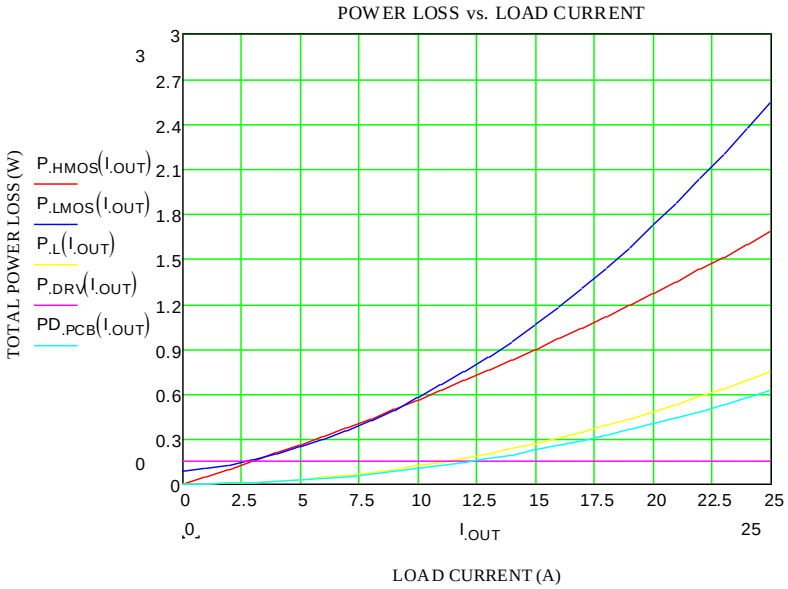

Figure 22. Key component loss in buck converter

Figure 23 shows detail component loss in buck converter and illustrates the loss v.s Iout in the curve.

HMOS : P_{HSW} (Switching loss) and P_{HCOD} (Conduction loss)

LMOS : P_{LCOD} (Conduction loss), P_{L_DIODE} (Dead-time body diode loss) and P_{RR} (Reverse recovery loss)

Inductor : P_L (Inductor DC & core loss)

Driver : P_{DRV} (Gate driver charge loss)

PCB : P_{PCB} (PCB trace loss)

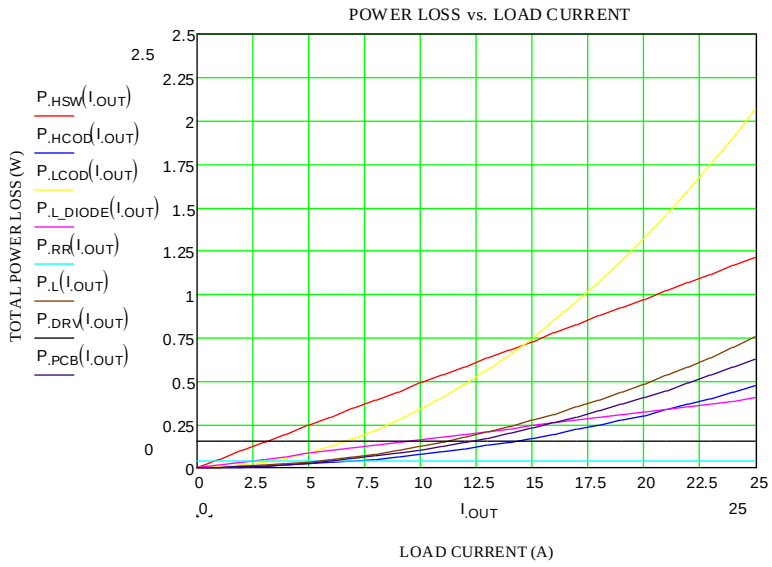

Figure 23. Detail power loss in buck converter

4. Conclusion

This application document analyzes power loss in synchronous buck converters and presents the detailed calculations for each part of the power loss. The loss calculation also compares with real buck converter measurement and provides the key component loss data to consider how to improve the buck converter efficiency for component and PCB plane consideration.

Reference

[1] Leon Chen, “Power Loss Analysis for Synchronous Buck Converter”, Application Engineer Dept data, 2013.

[2] Nelson Garcia, “Determining Inductor Power Losses”, Coil craft Document 486, 2005.

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: 886-3-5526789